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7

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/662,153	FRENGER ET AL.	
	Examiner	Art Unit	
	Ian N Moore	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-34 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-34 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4,5 .

4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: .

DETAILED ACTION

Notes/Remarks

1. It is noted that the "summary of the invention" is embedded within the "the background of the invention". It is suggested that the summary of the invention should be separated from the background.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4, 7-11, 14,22,23,31, and 32 are rejected under 35 U.S.C. 102(b) as being anticipated by Ayanoglu (U.S. 5,719,883).

Regarding Claims 1 and 9, Ayanoglu'883 discloses a method for use in data packet transmissions between a transmitter (see FIG. 1, Transceiver 20) and a receiver (see FIG. 1, Transceiver 30; see col. 3, line 34-47) where a data packet may include a first type/group of bits and a second type/group of bits (see col. 4, line 42-54 and col. 20, line 12-16; note that the data packet/word includes two types of parity checking bits: vertical parity bits/words (1) and information words/bits (2) which consist of informational bits and horizontal parity checking bits), the first type of bits/group being more important to decoding than the second type/group of bits (see col. 2, line 19-30; note that essential/importance of the parity bits/words can be either vertical or horizontal bits since the additional parity words/bits are

used to perform correction iterations in the receiver. The determination requirement of either the first/second type/group bits/words or both depends on the receiver. If these parity bits/words are important/essential for the receiver to decode, then those parity bits/words belong the first type/group.), and where a negatively acknowledged packet triggers a retransmission of the second type/group of bits to be used a subsequent decoding operation at the receiver (see col. 10, line 46-55; col. 19-37; and see FIG. 3D, step 410; note that when the receiver determines that the number of parity bits in the received block/data packet, it requests the transmitter to send/retransmit additional parity bits; thus, the requested packet for any particular parity bits (i.e. second type/group of bits) from the transmitter is the negatively acknowledged packet. The additional parity bits are used to determine and correct the received data/words. Also, note that the radio receiver performs additional decoding operation utilizing additional parity bits.), comprising:

decoding a received packet to produce an interim decoding result (see col. 2, line 12-19; the receiver detects and correct the error utilizing parity checking bits, and the receiver determines whether the result after the preliminary error correction is sufficient to correct all errors in the block/packet),

determining if the interim decoding result is above a threshold; detecting an absence of a data packet (see FIG. 3A, step 250; col. 2, line 1-19; col. 5, line 24 to col. 6 line 57; note the receiver detects errors by utilizing thresholds of the experiencing errors on the working channels; thus, the error is detected when either corrupted data packet or no data/packet is received.)

if the interim decoding result is not above the threshold, sending a lost signal; sending a lost signal to the transmitter rather than a negative acknowledgment (see FIG. 3A, step 250 and 290; col. 2, line 19-31; col. 5, line 24 to col. 6 line 57; col. 11, line 54-67; note that the receiver requests the retransmission when it detects that the running sum is higher than thresholds (i.e. working channel has transmission errors), or when there is no packet received within predetermined threshold/window interval. Note that loss of signal is the retransmission request.),

in response to the sending of the lost signal, receiving from the transmitter a first retransmission of the first type/group of bits of the data packet (see col. 2, line 32-50, col. 10, line 32 to col. 11, line 5; note that according to the request, the receiver receives the requested additional parity bits from the transmitter in the retransmission packet/data. Also, note that the first type/group of bits/words of the data packet can be any bits which are important to the receiver.); and

decoding the first retransmission (see col. 2, line 32-50; note that the receiver utilizes the addition bits to correct the errors during the decoding process in the radio receiver.)

Regarding Claims 2 and 31, Ayanoglu'883 discloses wherein the first type of bits includes actual information bits and the second type of bits includes parity bits (see FIG. 2, vertical parity checking bits and information and horizontal parity checking bits). See col. 10, line 45-65; note that receiver can request any specific bits from the transmitter as long as it receives the required bits. Thus, it is clear that the requested first type of bits can be either the information and horizontal parity checking bits or vertical parity checking bits; and similarly

requested second types of bits can be either vertical parity checking bits versa or the information and horizontal parity checking bits.

Regarding Claims 3, 10 and 32, Ayanoglu'883 discloses wherein the first retransmission also includes a first set of the second type of bits of the data packet (see FIG. 2; also see col. 10, line 45-65; note that receiver can request any specific bits from the transmitter (i.e. first retransmission request) as long as it receives the required bits. Thus, it is clear that the requested second types of bits can include either the vertical parity checking bits, or information and horizontal parity checking bits.

Regarding Claims 4 and 11, Ayanoglu'883 discloses if the decoding of the first retransmission is not successful (see FIG. 3D, Step 460; see col. 11, line 6-44; note that the receiver detects and unable to correct errors in the retransmission block/packet/data),

sending a negative acknowledgment to the transmitter (see FIG. 3D, Step 480; see col. 11, line 6-44; note that the receiver requests the specific bits from the transmitter);

receiving from the transmitter a second retransmission including a second set of the second type of bits different from the first set (see FIG. 3D, Step 420; see col. 11, line 6-44; also see col. 10, line 45-65; note that receiver can request any specific bits from the transmitter. Thus, it is clear that the specific requested bits in the second retransmission packet/word are either vertical/horizontal/informational bits or combination of bits (i.e. second type of bits), which are not the same bits from the first retransmitted bits.)

decoding the data packet using information from the first and second retransmissions (see FIG. 3D, Step 420-480; see col. 11, line 6-44; note that the step 420-480 are performed until the retransmission block/data/packet is correctly transmitted, and the receiver stores the results from each iteration (i.e. first and second retransmissions) in the memory for the decoding/processing utilizing parity and/or information bits.)

Regarding Claim 7, Ayanoglu'883 discloses wherein the packet is detected as absent by determining that a packet with a particular identifier expected to be received was not received in an expected time period (see FIG. 3A, step 210, 220, 235, 240,250; col. 2, line 1-19; col. 5, line 24 to col. 6 line 67; note the receiver determines if the block/packet is received within predetermined time interval and detects errors by utilizing experiencing errors thresholds on the working channels; thus, the error is detected when there is no data/packet received, or a receiver (i.e. processor) is experiencing a multi-path fading error in the particular channel. Multi-path fading error leads to the loss of data.)

Regarding Claim 8, Ayanoglu'883 discloses wherein the packet is detected as absent by comparing a decoding result for the packet with a threshold (see FIG. 3A, step 250, 290 and see FIG. 3B, 300, 310 and 320; col. 2, line 1-19; col. 5, line 24 to col. 6 line 67; note the receiver detects errors by utilizing experiencing errors thresholds on the working channels and requests for retransmission for the parity for each failed block/data/packet. Then after, it performs error correction on those newly received retransmitted packet/block and compare to the threshold to determine if the error still exists in the sub-block/part/bits of the packet. The

decoded results are stored in the memory after each iteration. Thus, the status of not fully corrected packet/block/bit is the status of absent packet since the packet/block/bit has not yet fully decoded.

Regarding Claim 14, Ayanoglu'883 discloses an apparatus for use in a transmitter which transmits data over a communications channel (see FIG. 1, Transceiver 20), comprising:

a signal processor (see FIG. 1, Processor 26) configured to process data and generates corresponding systematic bits and parity bits (see col. 3, line 47 to col. 4, line 65; note that the data packet/word includes two types of bits: vertical parity bits/words, and information words/bits which consist of informational bits and horizontal parity checking bits);

a combiner (see FIG. 1, the combined system of Processor 26 and memory 28) configured to selectively receive systematic and parity bits and generate a coded data packet (see transmitted parity checking bits in FIG. 2 and col. 3, line 47 to col. 4, line 41; note that the combined system of processor and memory selectively processes/generates different types of parity bits/words (i.e. vertical/horizontal parity bits and/or information bits) and transmit the data over the air);

transceiving circuitry (see FIG. 1, a combined system which consists of Receiver RECV 24 and Transmitter XMIT 22 of transceiver 20) configured to transmit coded data packets over the communications channel (see col. 3, line 34-65; note that since Transceiver 230 is the radio transmitter, it must transmit coded data over the air);

a controller (see FIG. 1, the combined system of Processor 26 and memory 28) configured to control which bits are selected by the combiner to generate the coded data packet based on feedback from a receiver (see col. 3, line 47 to col. 4, line 65; note the combined system of processor and memory also retransmits the requested and selected parity bits in the coded data/packet to the receiver),

wherein when a negative acknowledgment is received, parity bits are retransmitted over the communications channel to the receiver (see col. 2, line 19-30; col. 10, line 46-55; col. 19-37; and see FIG. 3D, step 410; note that essential/importance/type of the bits can be either vertical/horizontal parity bits, information bits, or the combination of bits since the additional bits are used to perform correction iterations at the receiver. The determination of which parity bits to request depends on the receiver. Thus, if the receiver determines that the number of incorrect bits in the received block/data packet, it requests the transmitter to send/retransmits specific additional parity bits; thus, a data/packet request for a specific parity bits (i.e. parity bits) from the transmitter is the negatively acknowledged packet.)

when a lost signal is received or no acknowledgment or negative acknowledgment is received, the systematic bits are retransmitted over the communications channel to the receiver (see col. 2, line 19-30; col. 10, line 46-55; col. 19-37; and see FIG. 3D, step 410; note that essential/importance/type of the bits can be either vertical/horizontal parity bits, information bits, or the combination of bits since the additional bits are used to perform correction iterations at the receiver. The determination of which bits to request depends on the receiver. Thus, after the receiver determines the number of incorrect bits in the received block/data packet, it requests the transmitter to send/retransmits specific additional bits. Note

that the receiver can request entire block of bits/word for retransmission. Thus, thus, a data/packet request for any specific bits (i.e. systematic bits) from the transmitter is the loss of signal/negatively acknowledged packet/non-acknowledgement packet.)

Regarding Claim 22, Ayanoglu'883 discloses an apparatus for use in a receiver which receives data over a communications channel (see FIG. 1, Transceiver 30), comprising:

transceiving circuitry (see FIG. 1, a combined system which consists of Receiver RECV 34 and Transmitter XMIT 32 of transceiver 30) configured to receive a coded data packet transmitted over the communications channel by a transmitter (see col. 3, line 34-47; note that since Transceiver 30 is the radio receiver, it must receive encoded/coded data over the air), where an initially transmitted coded data packet includes a first type of bits and a second type of bits (see col. 4, line 42-54 and col. 20, line 12-16; note that the data packet/word includes two types of bits: vertical parity bits/words, and information words/bits which consist of informational bits and horizontal parity checking bits), the first type of bits being more important to decoding than the second type of bits (see col. 2, line 19-30; note that essential/importance of the parity/informational bits/words can be either vertical/horizontal parity bits, information words/bits, or combination of bits since the additional words/bits are used to perform during correction/detection iterations in the receiver. The determination requirement of either the first/second type/group bits/words or both depends on the receiver. If these parity bits/words are important/essential for the

receiver to decode, then those parity bits/words belong the first type/group, which needs to be sent first);

packet processing circuitry (see FIG. 1, Processor 36) configured to detect the absence of an expected packet and to transmit a lost signal to the transmitter (see col. 2, line 1-19; col. 5, line 24 to col. 6 line 57; note the receiver detects errors by utilizing experiencing errors thresholds on the working channels; thus, the error is detected when either corrupted data packet or no data/packet is received.), and thereafter, to decode a first retransmission of the expected packet which includes the first type of bits (see col. 2, line 32-50, col. 10, line 32 to col. 11, line 5; note that according to the request, the receiver receives the requested additional bits from the transmitter in the retransmission packet/data. Also, note that the first type/group of bits/words of the data packet can be any bits, which are important to the receiver. Also, see col. 2, line 32-50; note that the receiver utilizes the addition bits to correct the error during the decoding process in the radio receiver.)

Regarding Claim 23, Ayanoglu'883 discloses wherein the packet processing circuitry includes: a decoder (see FIG. 1, the combined system of Processor 36 and MEM 38) for decoding a received data packet, and wherein if the data packet cannot be properly decoded (see col. 2, line 12-19; the receiver detects and correct the error utilizing parity checking bits, information bits, and/or both, and the receiver determines whether the result after the preliminary error correction is sufficient to correct all errors in the block/packet), a lost signal is sent to the transmitter (see FIG. 3A, step 250 and 290; col. 2, line 19-31; col. 5, line 24 to col. 6 line 57; col. 11, line 54-67; note that the receiver requests the retransmission

when it detects that the running sum is higher than thresholds (i.e. working channel has transmission errors), or when there is no packet received within predetermined threshold/window interval. Note that loss of signal is the retransmission request.)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 5,6,12,13, 17-21,29,30,33, and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ayanoglu'883 in view of well-established teaching in art.

Regarding Claims 5, 12 and 33, Ayanoglu'883 discloses wherein if the decoding of the first retransmission is not successful, a negative acknowledgment is send to the transmitter, and in response the second retransmission is received (see FIG. 3D, Step 460 and Step 480; see col. 11, line 6-44; note that when the receiver detects that it is unable to correct errors in the retransmission block/packet/data, it re-requests the specific bits from the transmitter). The second transmission includes any specific type of bits (see FIG. 3D, Step 420; see col. 11, line 6-44; also see col. 10, line 45-65; note that receiver can request any specific bits from the transmitter. The specific requested bits in the second retransmission packet/word are vertical/horizontal parity bits, information bits, or combination of bits, which may not include the same bits from the first retransmitted bits. The receiver will continue

requesting a specific bits until all erroneous bits in the packet/block are corrected, decoded, and transmitted.)

Ayanoglu'883 does not explicitly disclose wherein the second transmission does not include the first type of bits.

However, the above-mentioned claimed limitations are well known in the art. In particular, wherein the second transmission does not include the first type of bits. It is obvious that the receiver can specifically request second type of bits (i.e. not the first type of bits) since the first types of bits and corrected results are already stored in the memory. The second type bits of are required for correction and decoding for the remaining transmitted block/packet. Ayanoglu'883 teaches retransmitting any additional bits required to correct error in decoding. Thus, determining and selecting which bits, what type of bits, or various paring/combination of bits to retransmit are simply the matter of design choice since the <u>ultimate result</u> is to correct all errors in decoding process as taught by Ayanoglu'883.

In view of this, having the system of Ayanoglu'883 and then given the teaching in the art, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Ayanoglu'883, by requesting to send only the first type of bits, as taught by well established teaching in art. The motivation to combine is to obtain the advantages/benefits taught by Ayanoglu'883 (see col. 2, line 1-6) and well established teaching to reduce the number of ARQ retransmission by utilizing FEC correction and increase the throughput in the network since only specific bits are retransmitted other than entire data/packet.

Regarding Claims 6, 13 and 34, Ayanoglu'883 discloses wherein the second transmission includes any specific type of bits (see FIG. 3D, Step 420; see col. 11, line 6-44; also see col. 10, line 45-65; note that receiver can request any specific bits from the transmitter. The specific requested bits in the second retransmission packet/word are vertical/horizontal parity bits, information bits, or the combination of bits. The receiver will continue requesting for a specific bits until all erroneous bits in the packet/block are corrected, decoded, and transmitted.)

Ayanoglu'883 does not explicitly disclose wherein the second transmission includes the first type of bits and the second set of the second type of bits.

However, the above-mentioned claimed limitations are well known in the art. In particular, wherein the second transmission includes the first type of bits and the second set of the second type of bits. Ayanoglu'883 teaches retransmitting any additional bits required to correct error in decoding. Thus, determining and selecting which bits, what type of bits, or various paring/combination of bits to retransmit are simply the matter of design choice since the ultimate result is to correct all errors in decoding process as taught by Ayanoglu'883. Thus, both first and second type bits are required for correction and decoding for the remaining transmitted block/packet.

In view of this, having the system of Ayanoglu'883 and then given the teaching in the art, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Ayanoglu'883, by requesting to send both first and second type of bits, as taught by well established teaching in art. The motivation to combine is to obtain the advantages/benefits taught by Ayanoglu'883 (see col. 2, line 1-6)

and well established teaching to reduce the number of ARQ retransmission by utilizing FEC correction and increase the throughput in the network since the only required bits are retransmitted other than entire data/packet.

Regarding Claims 17, 18, 20, and 30, Ayanoglu'883 discloses wherein when a lost signal is received or no acknowledgment or negative acknowledgment is received (see FIG. 3D, Step 460 and Step 480; see col. 11, line 6-44; note that when the receiver detects that it is unable to correct errors in the retransmission block/packet/data, it re-requests the specific bits from the transmitter), then the requested specific bits are retransmitted over the communications channel to the receiver (see FIG. 3D, Step 420; see col. 11, line 6-44; also see col. 10, line 45-65; note that receiver can request any specific bits from the transmitter. The specific requested bits in the second retransmission packet/word are vertical/horizontal bits, information bits, or combination of bits, which may not include the same bits from the first retransmission. The receiver will continue requesting the specific bits until all erroneous bits in the packet/block are corrected, decoded, and transmitted.). Moreover, Ayanoglu'883 also discloses two types of bits: vertical parity bits, and information bits/words, which consist of information bits and horizontal parity checking bits. Thus, when re-transmitting, it is clear to resent the vertical parity bits along the information words/bits so that the receiver can fully correct and decode the block/packet.

Ayanoglu'883 does not explicitly disclose wherein the systematic bits are retransmitted over the communications channel to the receiver along with parity bits originally transmitted with the systematic bits; and wherein the systematic bits are

retransmitted over the communications channel to the receiver along with parity bits different from the parity bits originally transmitted with the systematic bits.

However, the above-mentioned claimed limitations are well known in the art. In particular, wherein the systematic bits are retransmitted over the communications channel to the receiver along with parity bits originally transmitted with the systematic bits; and wherein the systematic bits are retransmitted over the communications channel to the receiver along with parity bits different from the parity bits originally transmitted with the systematic bits. Both systematic and parity bits are required for correction and decoding for the remaining transmitted block/packet. Ayanoglu'883 teaches retransmitting any additional bits required to correct error in decoding. Thus, determining and selecting which bits, what type of bits, or various paring/combination of bits to retransmit are simply the matter of design choice since the ultimate result is to correct all errors in decoding process as taught by Ayanoglu'883. Thus, the transmitter may choose to retransmits original parity bits or non-original parity bits along with the systematic bits depending on what type/group/pair/combination of bits are being requested. Also, the receiver has a capability to store the corrected results in the memory (see Ayanoglu'883 FIG. 1, MEM 38), and the transmitter also has to a capability to store various types/combination parity bits and information bits in the memory (see Ayanoglu'883 FIG. 1MEM 28).

In view of this, having the system of Ayanoglu'883 and then given the teaching in the art, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Ayanoglu'883, by requesting to send both information and parity bits (both original and non-original), as taught by well established

teaching in art. The motivation to combine is to obtain the advantages/benefits taught by Ayanoglu'883 (see col. 2, line 1-6) and well established teaching to reduce the number of ARQ retransmission by utilizing FEC correction and increase the throughput in the network since the only required bits are retransmitted other than entire data/packet.

Regarding Claims 19, 21, and 29, Ayanoglu'883 discloses wherein when the systematic bits are retransmitted, and a negative acknowledgment signal is received in response to the retransmission (see FIG. 3D, Step 460 and Step 480; see col. 11, line 6-44; note that when the receiver detects that it is unable to correct errors in the retransmission block/packet/data, it re-requests the specific bits from the transmitter), any requested bits are retransmitted over the communications channel to the receiver (see FIG. 3D, Step 420; see col. 11, line 6-44; also see col. 10, line 45-65; note that receiver can request <u>any</u> specific bits from the transmitter. The specific requested bits in the second retransmission packet/word are vertical/horizontal parity bits, information bits, or combination of bits, which may not include the same bits from the first retransmission. The receiver will continue requesting the specific bits until all erroneous bits in the packet/block are corrected, decoded, and transmitted.)

Ayanoglu'883 does not explicitly disclose wherein in response to the retransmission, parity bits associated with the systematic bits are retransmitted over the communications channel to the receiver without the systematic bits.

However, the above-mentioned claimed limitations are well known in the art. In particular, in response to the retransmission, parity bits associated with the systematic bits are

retransmitted over the communications channel to the receiver without the systematic bits. Note that the systematic bits are utilized to detect/correct and the results are already stored in the memory. The parity bits are required for correction and decoding for the remaining transmitted block/packet. Ayanoglu'883 teaches retransmitting any additional bits required to correct error in decoding. Thus, determining and selecting which bits, what type of bits, or various paring/combination of bits to retransmit are simply the matter of design choice since the ultimate result is to correct all errors in decoding process as taught by Ayanoglu'883.

In view of this, having the system of Ayanoglu'883 and then given the teaching in the art, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Ayanoglu'883, by re-requesting to send only the parity bits, as taught by well established teaching in art. The motivation to combine is to obtain the advantages/benefits taught by Ayanoglu'883 (see col. 2, line 1-6) and well established teaching to reduce the number of ARQ retransmission by utilizing FEC correction and increase the throughput in the network since only specific bits are retransmitted other than entire data/packet.

4. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ayanoglu'883 in view of Eroz (U.S. 6,370,669).

Regarding claim 15, Ayanoglu'883 discloses the signal processor and combiner as a combined system as disclosed above in claim 14.

Ayanoglu'883 does not explicitly disclose using a turbo encoder.

However, the above-mentioned claimed limitations are taught by Eroz'669. In particular, Eroz'669 teaches discloses using a turbo encoder (see FIG. 2, Turbo code encoder 208; see col. 2, line 42 to col. 3, line 52 and see col. 6, line 19-52).

In view of this, having the system of Ayanoglu'883 and then given the teaching of Eroz'669, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Ayanoglu'883, by providing a turbo encoder, as taught by Eroz'669. The motivation to combine is to obtain the advantages/benefits taught by Eroz'669 since Eroz'669 states at col. 2, line 140 that such modifications would minimize implementation complexity and increase the redundancy scheme in the CDMA network.

Regarding claim 16, Ayanoglu'883 discloses the communication channel is the radio channel (see FIG. 1, system 10, a wireless system; col. 3, line 34-40; thus the communication channel must be the radio channel).

5. Claims 24 and 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ayanoglu'883 in view of Kalliojarvi (U.S. 6,438,723).

Regarding claim 24, Ayanoglu'883 discloses all aspects of the claimed invention set forth in the rejection of Claim 22 as described above, and further teaches the pack processing circuitry.

Ayanoglu'883 does not explicitly discloses a buffer for storing received data packet information; a combiner for combining buffer information with retransmitted information; a decoder for decoding an output of the combiner; and a controller coupled to the buffer, combiner, and decoder.

However, the above-mentioned claimed limitations are taught by Kalliojarvi'723. In particular, Kalliojarvi'723 teaches a buffer for storing received data packet information (see FIG. 6, RX Buffer 603);

a combiner for combining buffer information with retransmitted information (see FIG. 6, RX Buffer 603 which has combination functionality);

a decoder for decoding an output of the combiner (see FIG. 6, the combined decoding system of EC decoder 603 and ED decoder 605); and

a controller (see FIG. 6, the combined system of Retransmission Control 606 and Metrics Memory 604) coupled to the buffer, combiner, and decoder. Also, see col. 12, line 52 to col. 13, line 12.

In view of this, having the system of Ayanoglu'883 and then given the teaching of Kalliojarvi'723, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Ayanoglu'883, by providing detailed components of the processing unit, as taught by Kalliojarvi'723. The motivation to combine is to obtain the advantages/benefits taught by Kalliojarvi'723 since Kalliojarvi'723 states at col. 2, line 40-54 that such modification would increase good efficiency and acceptable robustness against error in the packet transmission.

Regarding claim 26, the combined system of Ayanoglu'883 and Kalliojarvi'723 discloses all aspects of the claimed invention set forth in the rejection of Claim 24 as described above, and Ayanoglu'883 further teaches the pack processing circuitry utilizing the adaptive ARQ/FEC techniques for transmission (see Ayanoglu'883 col. 1, line 49-64). Also,

Kalliojarvi'723 teaches that packet processor includes the buffer and the combiner. Thus, it is clear that the buffer and the combiner perform an incremental redundancy operation, which is performed by the redundancy scheme such as ARQ between the transmitter and receiver.

In view of this, having the system of Ayanoglu'883 and then given the teaching of Kalliojarvi'723, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Ayanoglu'883, by applying the ARQ redundancy operation in the buffer and combiner, as taught by Kalliojarvi'723 for the same motivation as stated above in claim 24.

Regarding claim 27, the combined system of Ayanoglu'883 and Kalliojarvi'723 discloses all aspects of the claimed invention set forth in the rejection of Claim 24 as described above, and Kalliojarvi'723 further teaches the decoder performs error correction (see FIG. 6, EC Decoder 603, i.e., error correcting decoder) and the packet processing circuit further detects errors in the output of the decoder. (See FIG. 6, ED Decoder, i.e., error detecting decoder at the output of the error correction decoder; and col. 12, line 52 to col. 13, line 12).

In view of this, having the system of Ayanoglu'883 and then given the teaching of Kalliojarvi'723, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Ayanoglu'883, by performing error correction and detection in the decoders, as taught by Kalliojarvi'723 for the same motivation as stated above in claim 24.

Regarding claim 28, the combined system of Ayanoglu'883 and Kalliojarvi'723 discloses all aspects of the claimed invention set forth in the rejection of Claim 24 as described above, and Ayanoglu'883 further teaches sending a negative acknowledgment signal to the transmitter. Kalliojarvi'723 also teaches wherein if the decoder output is not acceptable, the controller sends a signal to the transmitter (see FIG. 6, Retransmission Control and the ED Decoder 605; and col. 12, line 52 to col. 13, line 12; note that if the errors are detected after being corrected, they are forwarded to retransmission unit, and retransmission unit sends the request back to the transmitter unit).

In view of this, having the system of Ayanoglu'883 and then given the teaching of Kalliojarvi'723, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Ayanoglu'883, by sending a request/signal to the transmitter if erroneous data packet is detected after being corrected for retransmission, as taught by Kalliojarvi'723 for the same motivation as stated above in claim 24.

6. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ayanoglu'883 and Kalliojarvi'723 as applied to claim 22 and 24 above, and further in view of Eroz.

Regarding claim 25, the combined system of Ayanoglu'883 and Kalliojarvi'723 discloses all aspects of the claimed invention set forth in the rejection of Claims 22 and 24 as described above, and further teaches the decoder.

Neither Ayanoglu'883 nor Kalliojarvi'723 explicitly the decoder is a turbo decoder.

However, the above-mentioned claimed limitations are taught by Eroz'669. In particular, Eroz'669 teaches discloses using a turbo encoder (see FIG. 2, Turbo code encoder 232; see col. 2, line 42 to col. 3, line 52 and see col. 6, line 19-52).

In view of this, having the combined system of Ayanoglu'883 and Kalliojarvi'723, then given the teaching of Eroz'669, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Ayanoglu'883 and Kalliojarvi'723, by providing turbo decoder, as taught by Eroz'669. The motivation to combine is to obtain the advantages/benefits taught by Eroz'669 since Eroz'669 states at col. 2, line 140 that such modifications would minimize implementation complexity and increase the redundancy scheme in the CDMA network.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ian N Moore whose telephone number is 703-605-1531. The examiner can normally be reached on M-F: 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Ngo can be reached on 703-305-4798. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Ian N Moore
Examiner
Art Unit 2661

INM
1/15/03

RICKY NGO
PRIMARY EXAMINER